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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,278	YANG, JOON-HYUN	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1-3,14-18,22 and 23* is/are rejected.

7)☒ Claim(s) *4-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/09/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 22-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 recites "...providing current flow paths to generate predetermined driving voltage waveforms required for both X and Y axes electrodes according to predetermined switching sequences to drive the display panel". It is unclear what provides the current flow paths as claimed, and hence proper correction is needed.

Claim 23 is rejected by the virtue of its dependency on claim 22.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 14-15, 17-18, and 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Schermerborn (USPN 7081891).

Regarding claim 1, Schermerhorn teaches a single-sided driver *(Fig. 4 (30))* used with a display panel *(col. 4, lines 52-54, col. 6, lines 49-51, Fig. 4 (30, 14), a single driver circuit 30, which is capable of driving the a Plasma Display Panel (PDP) (14))*, the single-sided driver comprising: a single-sided driver circuit *(Fig. 4 (30))* having predetermined circuit elements including energy accumulation elements and switching elements *(col. 4, lines 52-67, col. 5, lines 1-48, Fig. 4 (28, 26, 32, 34, 44, 22), see components of driver circuit (30) in Fig. 4, first and second driver capacitors 22 and 44, first and second Injection Gate Bipolar Transistors (IGBT's) 32 and 34 that are sequentially switched between conducting and non-conducting states by a logic control circuit 39)*, and establishes current flow paths to generate predetermined driving voltage waveforms required for both X and Y axes electrodes according to predetermined switching sequences to drive the display panel *(col. 6, lines 8-18, Fig. 4 (17, 32, 26, 15), as shown in fig. 5, current through driver inductance 17 reaches a peak at t.sub.peak current after which the current begins to decrease as the voltage continues to rise, and the voltage reaches a peak at t.sub.reson; as shown in FIG. 5A, the operation continues through decision block 56 to functional block 58 where the first electronic switch 32 is returned to its non-conducting state at t.sub.off (fig. 5) with the voltage at the sustaining voltage level, and once the intended sustaining voltage is*

reached, it is held by the operation of the driver diode 26 and the PDP capacitors, see FIG. 5, which illustrates voltage and current waveforms generated by the driver circuit shown in FIG. 4, note that it is inherent that the PDP (14) shown in Fig. 4 has X and Y electrodes, col. 6, lines 1-2, also note as shown in Fig. 5, that at T.sub.start, the first electronic switch (32) is changed from a non-conducting state to a conducting state).

Regarding claim 14, Schermerhorn teaches method of designing a single-sided driver circuit *(Fig. 4 (30))* to drive a display panel *(col. 4, lines 52-54, col. 6, lines 49-51, Fig. 4 (30, 14), a single driver circuit 30, which is capable of driving the a Plasma Display Panel (PDP) (14), note that designing of the circuit (30) is inherent prior to its application)*, the method comprising: constructing the single-sided driver circuit including predetermined circuit elements having energy accumulation elements and switching elements *(col. 4, lines 52-67, col. 5, lines 1-48, Fig. 4 (28, 26, 32, 34, 44, 22), see components of driver circuit (30) in Fig. 4, first and second driver capacitors 22 and 44, first and second Injection Gate Bipolar Transistors (IGBT's) 32 and 34 that are sequentially switched between conducting and non-conducting states by a logic control circuit 39, note that the transistors (32, 34) and the capacitors (22, 44) and the rest of the components are all parts of a single driver circuit 30 as shown in Fig. 4, and constructing the circuit (30) is inherent prior to its application)*, wherein the

circuit elements are arranged so as to establish current flow paths to generate predetermined driver voltage waveforms that are required for X and Y axes electrodes of the display panel according to predetermined switching sequences to drive the display panel *(col. 6, lines 8-18, Fig. 4 (17, 32, 26, 15), as shown in fig. 5, current through driver inductance 17 reaches a peak at t.sub.peak current after which the current begins to decrease as the voltage continues to rise, and the voltage reaches a peak at t.sub.reson; as shown in FIG. 5A, the operation continues through decision block 56 to functional block 58 where the first electronic switch 32 is returned to its non-conducting state at t.sub.off (fig. 5) with the voltage at the sustaining voltage level, and once the intended sustaining voltage is reached, it is held by the operation of the driver diode 26 and the PDP capacitors, see FIG. 5, which illustrates voltage and current waveforms generated by the driver circuit shown in FIG. 4, note that it is inherent that the PDP (14) shown in Fig. 4 has X and Y electrodes, col. 6, lines 1-2, also note as shown in Fig. 5, that at T.sub.start, the first electronic switch (32) is changed from a non-conducting state to a conducting state).*

Regarding claim 22, Schermerhorn teaches a computer readable medium including data to perform a method of to providing driving voltages required for X and Y axes electrodes of a display panel *(as best understood, col. 4, lines 6-7 col. 4, lines 9-10, storing energy within the B-field established in the transformer coils, and injecting*

the stored energy into the display panel, col. 6, lines 16-18, Fig. 5 (lower solid line), and once the intended sustaining voltage is reached, it is held by the operation of the driver diode 26 and the PDP capacitors, see FIG. 5, which illustrates voltage and current waveforms generated by the driver circuit shown in FIG. 4, note that it is inherent that the PDP (14) shown in Fig. 4 has X and Y electrodes.), the method comprising: providing current flow paths to generate predetermined driving voltage waveforms required for both X and Y axes electrodes according to predetermined switching sequences to drive the display panel *(col. 6, lines 8-18, Fig. 4 (17, 32, 26, 15), as shown in fig. 5, current through driver inductance 17 reaches a peak at t.sub.peak current after which the current begins to decrease as the voltage continues to rise, and the voltage reaches a peak at t.sub.reson; as shown in FIG. 5A, the operation continues through decision block 56 to functional block 58 where the first electronic switch 32 is returned to its non-conducting state at t.sub.off (fig. 5) with the voltage at the sustaining voltage level, and once the intended sustaining voltage is reached, it is held by the operation of the driver diode 26 and the PDP capacitors, see FIG. 5, which illustrates voltage and current waveforms generated by the driver circuit shown in FIG. 4, note that it is inherent that the PDP (14) shown in Fig. 4 has X and Y electrodes, col. 6, lines 1-2, also note as shown in Fig. 5, that at T.sub.start, the first electronic switch (32) is changed from a non-conducting state to a conducting state).*

Regarding claims 2, 15 and 23, Schermerhorn teaches the single-sided driver circuit repeatedly supplies zero voltage and +/- multi-level voltages that are symmetric with respect to the zero voltage across the X and Y axes electrodes of the display panel during a sustain discharge period *(col. 4, lines 58-61, col. 5, lines 13-17, Fig. 5 (32, 34, A), as shown in Fig. 4, the driver circuit (30) includes transistors (32, 34) such that the cathode of the second IGBT 34 is connected to the negative terminal of a series combination of two variable voltage supplies 40 and 42 while the anode of the first IGBT 32 is connected to the positive terminal of the combined voltage supplies 40 and 42, wherein the transistors (32, 34) are sequentially switched between conducting and non-conducting states, col. 5, lines 66-67, the voltage at the PDP input port A is at ground or zero potential, note from Fig. 4 that the first IGBT 32 the second IGBT 34 are symmetrical with respect to input port A., col. 6, lines 16-18, as shown in fig. 5 (which shows voltage from time, t.sub.start to time, t.sub.off), at t.sub.off , the voltage is at a sustaining level, and a after reaching the sustaining voltage level, it is held by the operation of a driver diode (26) and PDP capacitors (15)).*

Regarding claim 17, Schermerhorn teaches the single-sided driver circuit is designed to have a capacitor clamp-type multi-level converting circuit structure *(see fig. 4, where a*

single driver circuit 30 includes capacitors (22,44), col. 5, lines 41-43, the first driver capacitor (22) is connected to ground while the second driver capacitor (44) is connected to the voltage feedback point (24), col. 5, lines 17-22, col. 6, lines 38-44, note that when the driver capacitor (44) is charged, the logic control (39) adjusts the voltage levels for next cycle, and the voltage supplies (40, 42) are connected and controlled by the logic circuit (39) such that the voltage supplies (40, 42) could be flyback transformers, also note that designing of the circuit (30) including its elements, capacitors (22, 44) is inherent prior to its application).

Regarding claim 18, Schermerhorn teaches the capacitor clamp-type multi-level converting circuit structure is designed by: connecting a plurality of capacitors in series *(see Fig. 4 in which, the first driver capacitor 22 is aligned on the same line as the second driver capacitor (44);* connecting the series of the capacitors between ground and a source voltage to be supplied to a sustain driver circuit *(see Fig. 4 in which the two capacitors (22, 44) are located between the ground and logic control (39, which controls voltage supplies 40 and 42) via feedback point (24))*; and connecting each of connection nodes of the capacitors to each of switching elements *(see Fig. 4 in which the capacitor (44) has two nodes each connected to elements, (26) and (32), and capacitor (22) has two nodes each connected to elements (34) and (28))* ; and repeatedly supplying zero voltage, and +/- multi-level

voltages that are symmetric with respect to the zero voltage, to the display panel during a sustain discharge period, by changing current flow paths according to the predetermined switching sequences to drive the display panel *(col. 4, lines 58-61, col. 5, lines 13-17, the cathode of the second IGBT 34 is connected to the negative terminal of a series combination of two variable voltage supplies 40 and 42 while the anode of the first IGBT 32 is connected to the positive terminal of the combined voltage supplies 40 and 42, such that the transistors (32, 34) are sequentially switched between conducting and non-conducting states, col. 5, lines 66-67, the voltage at the PDP input port A is at ground or zero potential, note from Fig. 4 that the first IGBT 32 the second IGBT 34 are symmetrical with respect to input port A., col. 6, lines 16-18, as shown in fig. 5 (which shows voltage from time, t.sub.start to time, t.sub.off), at t.sub.off , the voltage is at a sustaining level, and after reaching the sustaining voltage level, it is held by the operation of a driver diode (26) and PDP capacitors (15), col. 6, lines 8-18, Fig. 4 (17, 32, 26, 15), as shown in fig. 5, current through driver inductance 17 reaches a peak at t.sub.peak current after which the current begins to decrease, as shown in FIG. 5A, the operation continues through decision block 56 to functional block 58 where the first electronic switch 32 is returned to its non-conducting state at t.sub.off (fig. 5), also note as shown in Fig. 5, that at T.sub.start, the first*

electronic switch (32) is changed from a non-conducting state to a conducting state).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schermerhorn (USPN 7081891).

Regarding claims 3 and 16, Schermerhorn teaches as shown by the lower solid curve in FIG. 5, the voltage increases at a faster rate since the voltage supplies (40, 42) are set for higher outputs, and the voltage supplies (40, 42) are connected to and controlled by the logic control (39). Schermerhorn further teaches the voltage levels are set in function block (52) at a higher level to cause an injection of additional energy during a transition, and because of the increased energy, a plasma discharge is established at t.sub.discharge after which the sustaining voltages are maintained at t.sub.off (col. 6, lines 33-46, col. 5, lines 20-21, Fig. 4 (40,

42, 39), Fig. 5A (52)). ***Setting of the voltage outputs for voltage suppliers (40, 42) is dynamic such that the voltage levels can be set much higher (col. 6, lines 38-44).***

Schermerhorn does not specifically teach a source voltage to be supplied to the single-sided driver circuit is set to be twice as much as a voltage that is supplied to the display panel during a gas discharge mode in the sustain discharge period.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize Schermerhorn's logic control (39) (which sets higher levels through voltage supplies (40, 42)) for the purpose of determining the energy requirement to establish the desired plasma discharge as taught by Schermerhorn (col. 6, lines 27-29).

Allowable Subject Matter

7. Claims 19-21 are allowed.

Reasons for Allowance

8. The following is an examiner's statement of reasons for allowance:

Schermerhorn teaches a single driver circuit 30, which is capable of driving a plasma display panel (PDP) as shown in fig. 4 including first and second driver capacitors 22 and 44, first and second Injection Gate Bipolar

Transistors (IGBT's) 32 and 34 that are sequentially switched between conducting and non-conducting states by a logic control circuit 39, and the voltage and current waveforms generated by the driver circuit (30) as shown in Fig. 5, which includes time, t.sub.off at which the sustaining voltage level is reached (col. 4, lines 52-67, col. 5, lines 1-26, Fig. 4 (30, 22, 44, 32, 34, 39)).

Regarding claim 19, Schermerhorn does not teach single-sided driver circuit to drive X and Y electrodes of a display panel, comprising: an isolation and reset circuit combination to establish a current flow path to generate reset ramp voltage waveforms for the X and Y axes electrodes to eliminate wall charges on the display panel while cutting off the energy recovery path during a reset period; a scan pulse generation circuit connected with the isolation and reset circuit combination and the X and Y axes electrodes to establish a current flow path to generate voltage waveforms for the X and Y axes electrodes to make wall charges on the display panel during an address period; and a sustain driver circuit connected with the isolation and reset circuit combination and the X and Y axes electrodes to establish charging/discharging paths to charge/discharge the display panel according to predetermined switching sequences to drive the display panel during the sustain discharge period, and to establish predetermined current flow paths to generate a reset voltage waveform and an address discharge voltage waveform in combination with the reset circuit and the scan pulse generation circuit, respectively, during the reset period and the address period.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Claims 4-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Schermerhorn teaches a single driver circuit 30, which is capable of driving a plasma display panel (PDP) as shown in fig. 4 including first and second driver capacitors 22 and 44, first and second Injection Gate Bipolar Transistors (IGBT's) 32 and 34 that are sequentially switched between conducting and non-conducting states by a logic control circuit 39, and the voltage and current waveforms generated by the driver circuit (30) as shown in Fig. 5, which includes time, t.sub.off at which the sustaining voltage level is reached (col. 4, lines 52-67, col. 5, lines 1-26, Fig. 4 (30, 22, 44, 32, 34, 39)).

Regarding claim 4, Schermerhorn does not teach a single-sided driver including a single a single -sided driver circuit comprising an isolation and reset circuit combination which isolates an energy recovery path and establishes a current flow path to generate reset voltage waveforms that are supplied to both the X and Y axes electrodes to eliminate wall charges in the display panel during a reset period; a scan pulse generation circuit which establishes a current flow path to generate address discharging voltage waveforms to be supplied to the X and Y axes electrodes to generate wall charges in the display panel during an address period; a sustain driver circuit which establishes charging/discharging paths to charge/discharge the display panel according to the predetermined switching sequences to drive the display panel during a sustain discharge period, and establishes a current flow path to generate the reset voltage waveform and the address discharging voltage waveforms during the reset period and the address period, respectively, in combination with the isolation and reset circuit and the scan pulse generation circuit.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts re cited for further reference.

U.S. Pat. No. 6,906,706 to Kosaka et al. teach as shown in Fig. 3 a drive unit 21, which includes a controller (31) and a power source circuit 41 such that the driver unit 21 is used for controlling potential of scan electrodes S.sub.1 -S.sub.N and data electrodes A.sub.1 -A.sub.M.

U.S. Pat No. 7,190,337 to Miller et al teach that by configuring the EIOs and R/C's independently, a single driver can support 16 row.times.64 column, 32 row.times.48 column, 48 row.times.32 column, and 64 row.times.16 column (col. 6, lines 43-45).

U.S. application No. 20020000955 to Derken et al teach . as shown in Fig. 14A & 14 B sub-electrodes 141 Y1, 142 X1 at opposite sides of the panel are interconnected and a single driver circuit (144) is used to drive the electrodes.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas I Abdulselam
Examiner
Art Unit 2629
May 9, 2007